Turning now to each of the cited references, Assaderaghi et al. (U.S. Pat. No. 5,811,857), is directed to a type of diode circuit implemented from a SOI field effect transistor. As illustrated in Fig. 1, an FET is fabricated and the gate and drain connections are in turn connected to the body connection. The terminal being protected is connected at point B.

As is the case with ESD circuits, the diode serves to limit any potential which may occur as a result of an electrostatic discharge to point B, by rapidly discharging the electrostatic potential through the diode created by FET 10.

The application for the created diode is shown in Figs. 9-20. In each of the figures, a input pad 68 is connected via two FET diodes 64 and 66 to V_1 and V_2. In this way, either a high positive or negative electrostatic potential may be rapidly dissipated through diode 64 and 66 to terminals V_1 and V_2.

The present invention is not directed to an apparatus or device for protecting a circuit from a electrostatic charge. The function of the method in accordance with the rejected claims is to move any preexisting accumulated charge on the body of an SOI device prior to operating, or accessing, that device. The claimed method requires that prior to accessing the device, a discharge of the body of the device occur to remove any accumulated charge.

The process as set forth in the steps of the rejected claims does not describe a ESD protection device. In an ESD protection, it is not potential or charge on the body of a device which is lowered, but the potential on a input terminal or a pad resulting from an inadvertent electrostatic discharged so that it does not ever reach a level which can damage the device. Accordingly, the steps as recited in Applicants rejected claims cannot be read on an ESD event described in the cited patent, since there is no lowering of the charge on the SOI device body.

Withdrawal of the rejection of claims 6-14 as being anticipated by Voldman (U.S. Pat. No. 6,074,899), is requested. Voldman describes another type of ESD device where an ESD protection network is incorporated in the bulk of the silicon and the SOI film of an integrated circuit device. The embedded ESD networks are located beneath the active core circuitry of an integrated circuit device. The result is an ESD protection which avoids the problem of a high perimeter gate structures of an ESD network constructed in a three-dimensional SOI structure.

The ESD network provides for protection from a high, electrostatic potenti l which may inadvertently be connected to an exterior connection of an input pin/pad. The reference descries how these electrostatic events are shunted to a lower potential, but fails to disclose or suggest any process or motivation for a process which would reduce the charge accumulation on the body of an SOI device, prior to activating that device. Each of Applicants claims have been amended to include the method limitation that the body is discharged prior to accessing the device. The purpose, is not to protect the device from an electrostatic event, but to enhance performance of the device by removing any accumulated charge on the body.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a 35 U.S.C. 102 rejection. See MPEP 2131.

The present claims include a method limitation not disclosed in either cited reference. This method limitation requires that prior to accessing an SOI device, the charge on the SOI body be removed. It is submitted that if the current rejections are to be maintained, that the Examiner point-out where in either reference one can find this limitation.

The Office Action states that Vodlman (U.S. Pat. No. 6,074,899) discloses at col. 4, line 67 a pulse generator to generate a pulse. However, reviewing the patent at this location fails to disclose any such pulse generator.

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As it has been demonstrated that the claims as amended contain the limitations not found or suggested in the various references dealing with ESD protection, as distinguished from enhancing circuit performance by discharging body potential, the references do not anticipate or render obvious the subject matter of these claims.

In view of the foregoing, favorable reconsideration is requested.

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Respectfully submitted,

By _____

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MARKED-UP REVISIONS

IN THE CLAIMS:

9. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

selectively grounding the body of at least one of the plurality of SOI devices to dissipate an electric charge accumulated in the body of the at least one of the plurality of SOI devices before accessing said SOI devices.

11. (Amended) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator connected to the circuit;

using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator prior to accessing said at least one SOI devices.